What is claimed is:

1. A method of filling a bit line contact via, comprising:

providing a substrate having a device region and periphery region, the device region having a transistor with a gate electrode, drain region, and source region on the substrate;

forming a dielectric layer overlying the substrate, the dielectric layer having a bit line contact via exposing the drain region, and periphery contact via exposing the periphery region;

forming a doped conductive layer, lower than the dielectric layer, overlying the drain region;

conformally forming a barrier layer overlying the dielectric layer, doped conductive layer, and periphery region; and

forming a first conductive layer filling the bit line contact via and periphery contact via.

2. The method as claimed in claim 1, wherein the dielectric layer is oxide.

3. The method as claimed in claim 1, wherein the doped conductive layer is polycrystalline silicon doped with As.

4. The method as claimed in claim 1, wherein forming the doped conductive layer further comprises:

forming the doped conductive layer overlying the drain region, dielectric layer, and periphery region; and

removing the doped conductive layer by etching, thereby leaving a doped conductive layer overlying the drain region.

5. The method as claimed in claim 1, wherein the barrier layer prevents the diffusion of the first conductive layer.

6. The method as claimed in claim 1, wherein the barrier layer comprises a TiN layer.

7. The method as claimed in claim 1, wherein the first conductive layer is tungsten.

8. The method as claimed in claim 1, wherein the periphery region is a doped region.

9. The method as claimed in claim 1, wherein the periphery region is a second conductive layer, and the gate electrode further comprises the second conductive layer.

10. The method as claimed in claim 9, wherein the second conductive layer is a silicide layer comprising tungsten.

11. A method of a filling bit line contact via, comprising:

providing a substrate having a device region and periphery region, the device region having a transistor with a gate electrode, drain region, and source region on the substrate;

forming a dielectric layer overlying the substrate, the dielectric layer having a bit line contact via

exposing the drain region, and periphery contact via exposing the periphery region;

forming a doped conductive layer overlying the drain region, dielectric layer, and periphery region;

removing the doped conductive layer using etching, thereby remaining the doped conductive layer, lower than the dielectric layer, overlying the drain region;

conformally forming a barrier layer overlying the dielectric layer, doped conductive layer, and periphery region; and

forming a first conductive layer filling the bit line contact via and periphery contact via.

12. The method as claimed in claim 11, wherein the dielectric layer is an oxide layer.

13. The method as claimed in claim 11, wherein the doped conductive layer is polycrystalline silicon doped with As.

14. The method as claimed in claim 11, wherein the barrier layer prevents the diffusion of the first conductive layer.

15. The method as claimed in claim 11, wherein the barrier layer comprises a TiN layer.

16. The method as claimed in claim 11, wherein the first conductive layer is tungsten.

17. The method as claimed in claim 11, wherein the periphery region is a doped region.

18. The method as claimed in claim 11, wherein the periphery region is a second conductive layer, and the gate electrode further comprises the second conductive layer.

19. The method as claimed in claim 18, wherein the second conductive layer is a silicide layer comprising tungsten.